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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,065	10/24/2005	Catherine Robert	S1022.81242US00	1848

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EXAMINER	
VICARY, KEITH E	
ART UNIT	**PAPER NUMBER**
2196	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,065	ROBERT ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are pending in this application. Claims 1-3 and 5-7 have been amended and claim 4 has been unchanged by amendment filed 5/13/2005. Claims 1-7 are presented for examination.

Specification

2. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

a. "www.ieee-isto.org/Nexus5001," page 2, line 13.

Claim Objections

3. Claims 1, 2, 5, and 7 are objected to because of lack of antecedent basis. Appropriate correction is required.

b. "the microprocessor," claim 1, line 2.

c. "the instruction," claim 1, line 6.

d. "the transmission," claim 1, line 7.

e. "the destination instruction address," claim 1, line 10.

f. "the last executed instruction," claim 2, line 3.

Claim Rejections - 35 USC § 112

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

g. "...the destination instruction corresponding to an instruction of a series of specific instructions which does not belong to the instruction series," claim 5, line 3. It is unclear as to how a destination instruction corresponding to an instruction of a series of specific instructions simultaneously does not belong to that instruction series as well. For the purposes of this office action, the examiner is reading the above to be "...the destination instruction corresponding to an instruction of a series of specific instructions which does not belong to the instruction sequence." Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Argade et al. (Argade) (US 5724505) in view of Nexus 5001 Forum: Standard for a Global Embedded Processor Debug Interface (Nexus 5001 Forum).

7. Argade is cited by the applicant in IDS paper filed 5/13/2005.

8. Nexus 5001 Forum is cited by the applicant in IDS paper filed 5/13/2005.

Consider claim 1, Argade discloses a method for transmitting digital messages (col. 6, lines 24-27, wherein the signal is the digital message; col. 6, lines 46-48, wherein the shifting to the JTAG interface is the first phase of transmittal; and col. 4, lines 63-65, wherein the movement into the JTAG port and the debug host computer is the second phase of transmittal), on execution of an instruction sequence by the microprocessor (col. 4, lines 30-31, 39; the program trace), through output terminals (col. 4, 59-65, JTAG interface and port) of a monitoring circuit (col. 4, lines 51, 59-65, HDS block) integrated to the microprocessor (col. 4, line 39; Figure 1 also shows the JTAG interface (24), JTAG port (44), and monitoring circuit (26) clearly inside the microprocessor (10)), at least one of said digital messages being representative of characteristic data stored by the monitoring circuit on detection of a jump in the execution of the instruction sequence from an initial instruction to a destination instruction different from the instruction following the initial instruction in the instruction sequence (col. 5, lines 39-45, wherein a discontinuity corresponds to the jump, and the INSTR_TYPE and its corresponding address is the characteristic data, which is part of the digital message as seen again in col. 6, lines 24-27), comprising, for the transmission of a digital message, the steps of:

determining whether the jump is associated with a jump instruction of the instruction sequence for which data representative of the destination instruction

address of the jump is explicitly indicated in the instruction (col. 5, lines 65-67, the third discontinuity type includes an absolute address instruction jump or call)

assigning to a second set of bits of the digital message a third value identifying the jump from among several types of jumps (col. 5, lines 39-45, the INSTR_TYPE, which is part of the digital message as above in col. 6, lines 24-27); and transmitting the digital message (col. 6, lines 24-27, wherein the signal is the digital message; col. 6, lines 46-48, wherein the shifting to the JTAG interface is the first phase of transmittal; and col. 4, lines 63-65, wherein the movement into the JTAG port and the debug host computer is the second phase of transmittal).

However, Argade does not disclose, after determining whether the jump is associated with a jump instruction of the instruction sequence for which data representative of the destination instruction address of the jump is explicitly indicated in the instruction; if yes, assigning a first value to a first set of bits of the digital message, and if not, assigning a second value to the first set of bits. Consequently, Argade also does not disclose, if the first set of bits is at the second value, assigning to a second set of bits of the digital message a third value identifying the jump from among several types of jumps.

On the other hand, Nexus 5001 Forum does disclose determining whether the jump is associated with a jump instruction of the instruction sequence for which data representative of the destination instruction address of the jump is explicitly indicated in the instruction; if yes, assigning a first value to a first set of

bits of the digital message, and if not, assigning a second value to the first set of bits (Table 6-6 and Table 6-7, with the T-codes analogous to "the first set of bits," and their values differing depending on whether it is a direct branch message or an indirect branch message).

Furthermore, the identifying of the jump of Argade, which includes identifying the jump as having an explicitly indicated destination instruction address, encompasses the identifying of the jump of the instant application, which tests for the explicitly indicated destination instruction address condition first before only identifying the jump if that test fails.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Argade with the teaching of having a specific field indicating whether the destination instruction address of the jump is explicitly indicated in the instruction of Nexus 5001 Forum in order to conform with IEEE standards.

Consider claim 7, Argade discloses a device for transmitting digital messages (col. 6, lines 24-27, wherein the signal is the digital message; col. 6, lines 46-48, wherein the shifting to the JTAG interface is the first phase of transmittal; and col. 4, lines 63-65, wherein the movement into the JTAG port and the debug host computer is the second phase of transmittal) between a monitoring circuit (col. 4, lines 51, 59-65, HDS block) integrated on a microprocessor (col. 4, line 39; Figure 1 also shows the JTAG interface (24),

JTAG port (44), and monitoring circuit (26) clearly inside the microprocessor (10)) and an analysis tool (col. 4, lines 59-65, debug host computer) via output terminals (col. 4, 59-65, JTAG interface and port) comprising:

means of detection of a jump on execution of an instruction sequence by the microprocessor (col. 5, lines 32-38, program trace, recording...details about the discontinuity; detection of the discontinuity is inherent in order to record details about it);

means for storing data characteristic of the detected jump (col. 6, lines 12-19, 43-46, INSTR_TYPE and ADDR data)

means for transmitting the determined digital message (col. 6, lines 24-27, wherein the signal is the digital message; col. 6, lines 46-48, wherein the shifting to the JTAG interface is the first phase of transmittal; and col. 4, lines 63-65, wherein the movement into the JTAG port and the debug host computer is the second phase of transmittal);

determination means capable of comprising a second set of bits in the digital message set to a third value identifying the jump from among several jump types (col. 5, lines 39-45, the INSTR_TYPE, which is part of the digital message as above in col. 6, lines 24-27).

However, Argade does not disclose means for determining a digital message based on the stored characteristic data, the digital message comprising a first set of bits set to a first value if the jump is associated with a jump instruction of the instruction sequence for which data representative of the

destination instruction address of the jump are explicitly indicated in the instruction, and set to a second value in the opposite case. Consequently, Argade also does not disclose, when the first set of bits is set to the second value, the determination means is capable of comprising a second set of bits in the digital message set to a third value identifying the jump from among several jump types.

On the other hand, Nexus 5001 Forum does disclose means for determining a digital message based on the stored characteristic data, the digital message comprising a first set of bits set to a first value if the jump is associated with a jump instruction of the instruction sequence for which data representative of the destination instruction address of the jump are explicitly indicated in the instruction, and set to a second value in the opposite case (Table 6-6 and Table 6-7, with the T-codes analogous to "the first set of bits," and their values differing depending on whether it is a direct branch message or an indirect branch message).

Furthermore, the identifying of the jump of Argade, which includes identifying the jump as having an explicitly indicated destination instruction address, encompasses the identifying of the jump of the instant application, which tests for the explicitly indicated destination instruction address condition first before only identifying the jump if that test fails.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Argade with the teaching of

having a specific field indicating whether the destination instruction address of the jump is explicitly indicated in the instruction of Nexus 5001 Forum in order to conform with IEEE standards.

Consider claim 2, the claim is rejected for same reasons as claim 1 above. In addition, Nexus 5001 Forum discloses the step of assigning to a third set of bits of the digital message a value corresponding to the number of instructions executed by the microprocessor since the last executed instruction of the instruction sequence corresponding to a digital message associated with a jump (page 59, Table 6-6 and 6-7, the I-CNT field).

Consider claim 3, Argade and Nexus 5001 Forum disclose the step of, if the first set of bits is at the second value, assigning to a fourth set of bits of the digital message a value representative of the address of the destination instruction (Argade, col. 5, lines 52-56 and Nexus 5001 Forum, Table 6-7, U-ADDR).

Consider claim 4, Argade discloses a jump type corresponds to a jump resulting from a jump instruction of the instruction sequence containing the

reference of a register in which are stored data representative of the destination instruction address (col. 5, lines 59-65).

Consider claim 5, Argade discloses a jump type corresponds to a jump forced by the microprocessor, the destination instruction corresponding to an instruction of a series of specific instructions which does not belong to the instruction series (col. 5, lines 49-52).

Consider claim 6, Argade discloses a jump type corresponds to a jump forced by the microprocessor, the destination instruction being an instruction of the instruction sequence (col. 5, lines 65-67 and col. 6, line 1; relative...address jump or call).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on 571-272-3963. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KV

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N. El-Hady

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SUPERVISORY PATENT EXAMINER